

Figure 1

Chu et al.
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 Method of Power Consumption
 Reduction in Clocked Circuits
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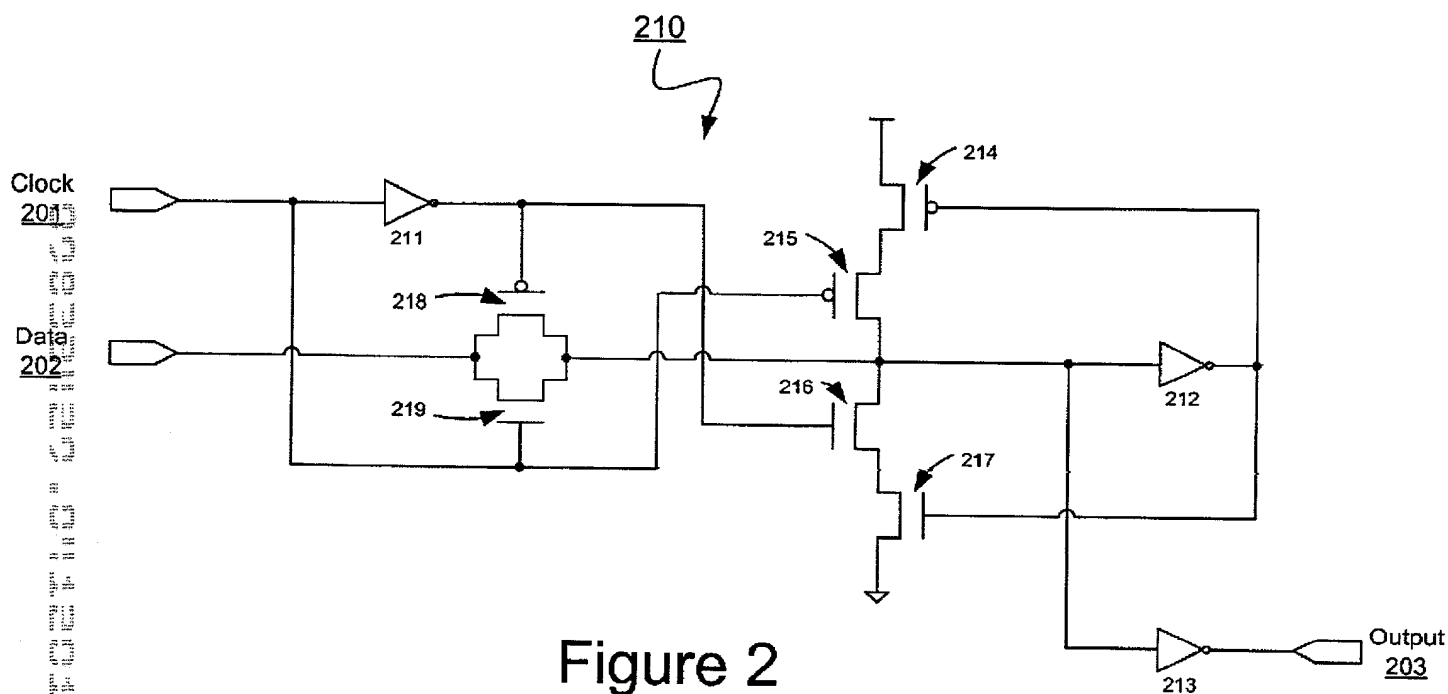


Figure 2

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Figure 3

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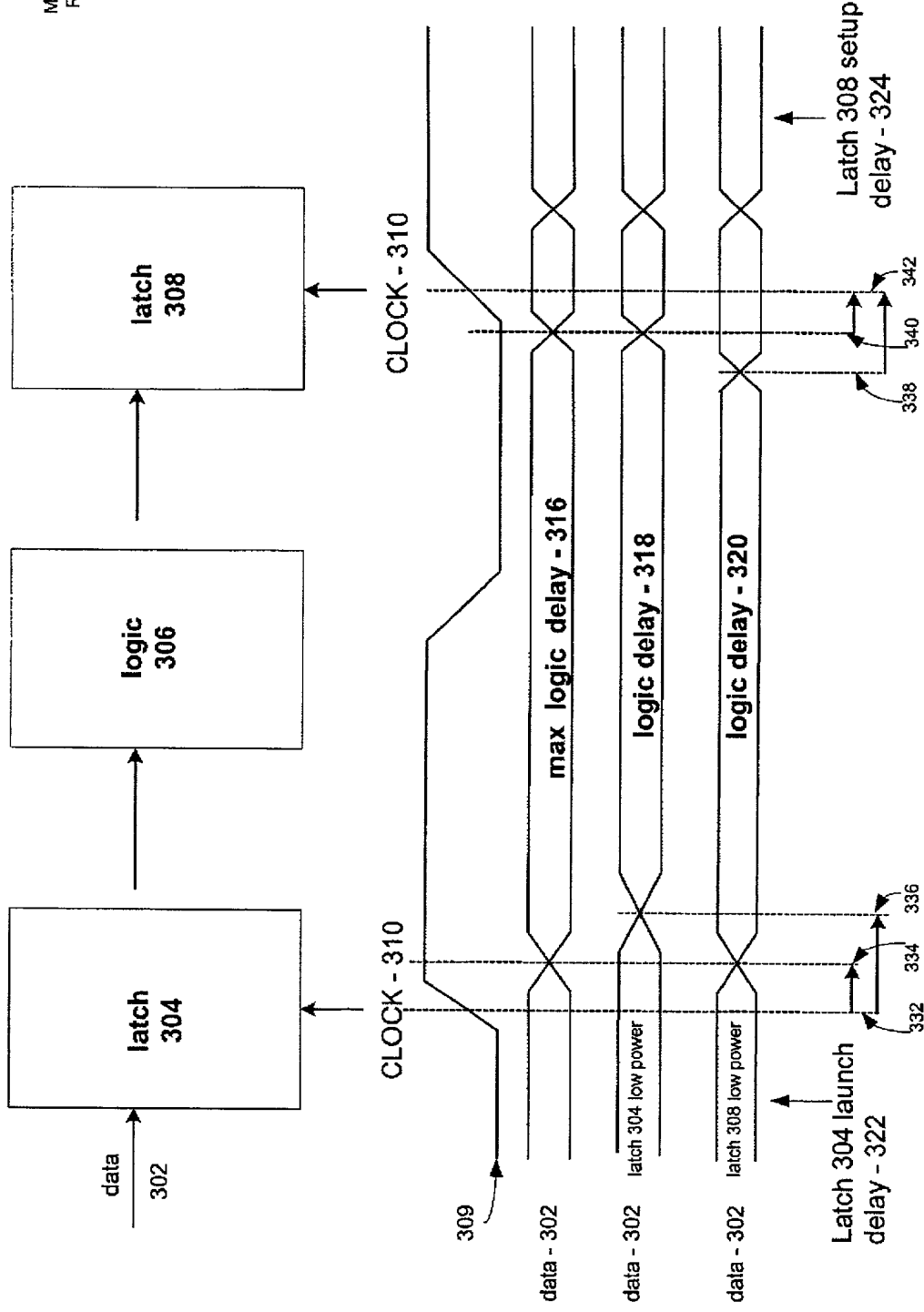


Figure 4

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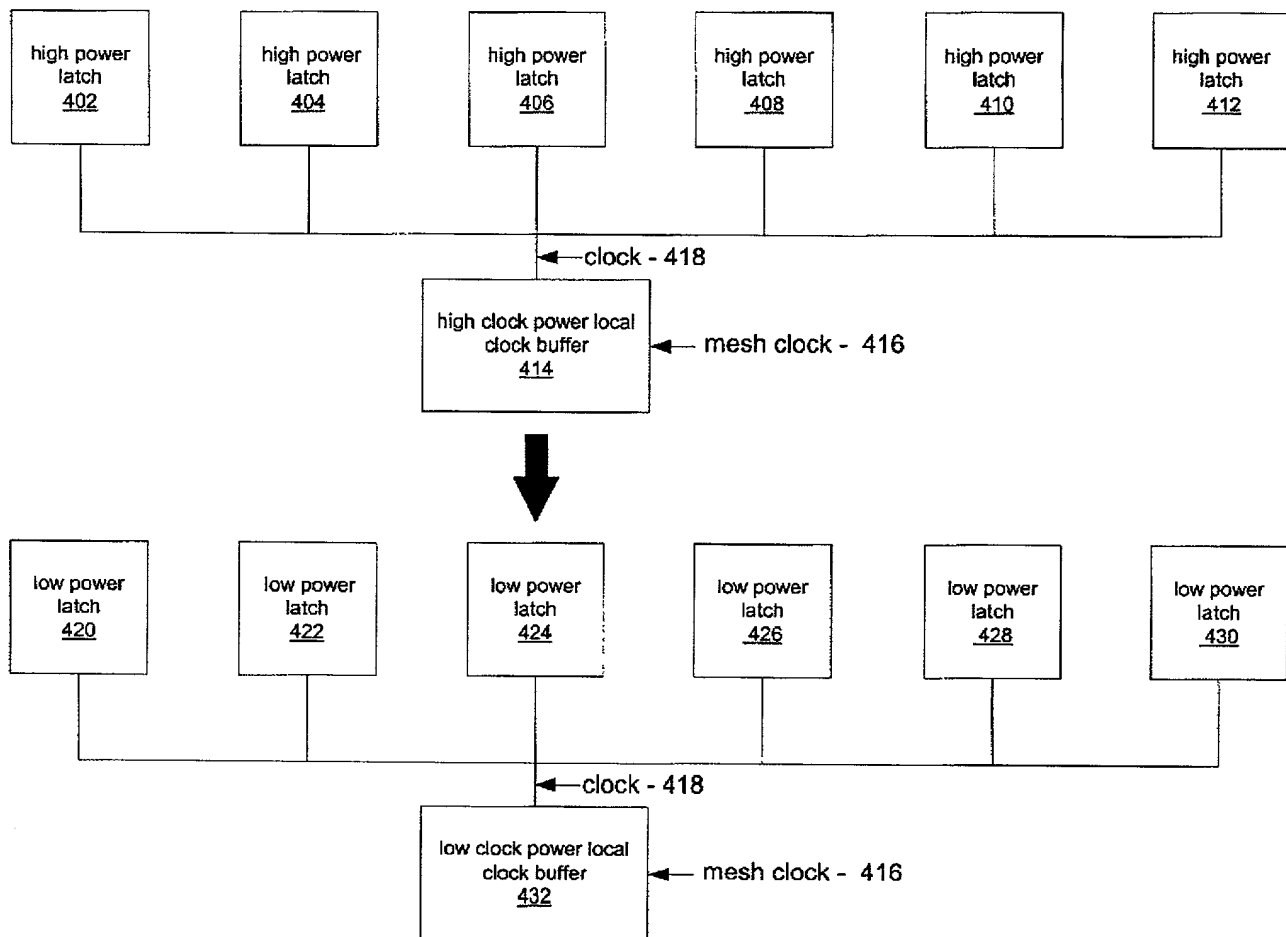


Figure 5

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